Model 305 Synchronous Countdown System

Introduction:
The Model 305 pre-settable countdown electronics is a high-speed synchronous divider that generates an electronic trigger pulse, locked in time with the input stimulus. The output trigger rate is integer related to the input clock rate by a six decade thumbwheel switch on the front panel. The primary application of this instrument is to provide all the required timing, delay, adjustments and output signals necessary to drive a variety of laser pulse selection modulation systems.

Technical Overview:
The countdown utilizes Emitter Coupled Logic (ECL) to insure minimal jitter and toggle rates in excess of 140MHz. This system will accept the sinusoidal output of the mode-locker oscillator or a detected analog of the optical pulse train exiting the laser as its input clock. The mode locker input is internally frequency doubled before it becomes the clock for the counter. The external input is 1/1.

There are three basic operating modes for the counter, CW, Gated and Single Shot. The CW mode outputs a continuous string of pulses with the division rate set by the thumbwheel. The Gated mode outputs a burst of pulses, the rate of the number of pulses in the burst is set by the thumbwheel and the width or number of pulses within the burst is controlled by a TTL pulse applied to the gate input of the instrument. The Single Shot mode outputs a single pulse in response to the leading edge of a TTL signal applied to the S.S. input. This input enables the counter to generate a single output pulse after it has divided the clock by the thumbwheel setting. The output pulse is therefore delayed in time from the TTL Single Shot input by the setting of the thumbwheel and the input clock rate. The counter automatically resets itself after the pulse is generated. In all operating modes, the timing of the counter is tied only to the input clock, the external mode inputs (Gate or Single Shot) simply enable the event to occur.

There are three outputs generated by the system, a High Speed Analog Output, TTL Output and a Line Sync Out. The High Speed Analog Output is capable of operating up to 70MHz output rates. The TTL Out will deliver output rates in excess of 1MHz. The Line Sync is capable over the full range of the instrument. All outputs are designed to drive a 50ohm load.
The instrument has an 8ns variable delay along with a 8ns fixed (in/out) delay. The variable delay element is a 7-bit digital delay line with a linear front panel control. This delay feature yields a total of 16ns of adjustment with a minimum resolution of 62ps. The delay may be locked once the appropriate setting is obtained. Sixteen (16ns) of variable delay insures alignment of the electrical output of the instrument to the optical pulse down to C/2L rates of 63MHz. No further delay adjustments in the overall system are required.

**Model 305 Specifications:**

<table>
<thead>
<tr>
<th>Input Clock Rate</th>
<th>Mode Locker Input, 10MHz Min, 70MHz Max</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>External Input, 10Hz min, 140MHz Max</td>
</tr>
<tr>
<td>Countdown Range</td>
<td>F(clock)/2 min, f(clock)/1*10^6 max</td>
</tr>
<tr>
<td>Input-Output Jitter</td>
<td>&lt;100ps, any count</td>
</tr>
</tbody>
</table>

**Input Requirements**

1. Mode Locker Input – sine wave, -6dbm min (112mv RMS), +15dbm, ax (1.3v RMS), Zi=50ohms
2. External Input – 100mv peak min, 1.5ns min pulse width. +/- 2v peak max. Zi=50ohms
3. Gate Input = TTL levels, min width one clock period. Burst ends one count after negative edge of gate input signal. Zi=50ohms
4. Single Shot Input = TTL levels, 10ns min pulse width. Zi=50ohms.

**Delay**

Variable – 0-to-8ns, 7bit digital delay line. 62ps min resolution. Controlled by linear, single turn front panel control. Fixed – 8ns Switch selectable on front panel (in/out)

**Outputs**

TTL – 50 ohm line driver, Voh type 2.5v into 50ohm load. Pulse width 1us type (Pulse with is set internally by discrete components). Tr, Tf, <3ns type

Analog – Tr, Tf, <2ns, Unipolar 0-to-+1v fixed amplitude. Designed to drive DC coupled 50ohm load to ground. Pulse width – 8ns, set internally by 50ohm coax delay line.

Sync – 50ohm TTL line driver, 1.3v into 50ohms. Negative edge.

**Threshold Adjustment**

+/- 200mv applied to input comparator via single turn front panel control.

**Input Power**

85-250VAC, 47-63Hz, 50W

**Dimensions**

133 H x 430 W x 343 D mm. Rack Mountable. 5.25” x 16.88” x 13.5”

**Weight**

Net 6.8 Kg, (15lbs)
**Interface and Operating Instructions**

There are two types of operational modes the Model 305 will typically be used in.

1. **Mode Locker Input.**
   This mode takes a sample of the electrical signal generated by a Mode Locker Oscillator; frequency doubles it and translates the signal to ECL logic levels to drive the clock line of the counter.

2. **External Input.**
   This mode will typically be a detected analog of the optical pulse train exiting the laser. High speed PIN or avalanche photo-detectors would be used to convert the laser output to an electrical signal. This input is then directly converted to ECL to drive the clock line of the counter.

**Mode Locker Input:**
The Mode Locker input is designed to accept the electrical signal from the oscillator directly. Certain level requirements on this signal must be verified before the signal is connected to the instrument. The input level into a 50ohm load must be a minimum of -6dbm (112mv RMS) in amplitude and be between 10MHz and 70MHz. The input level may be greater than -6dbm but should be less than +15dbm (1.3v RMS) to avoid damage to the front end of the system. An external 50ohm attenuator should be used to reduce this level if required.

Connect the Model Locker signal to the BNC connector marked “Mode Locker”. Place the “Threshold” control to mid-range and adjust the “Level” control to obtain a “green” indication on the level LED. Monitor the analog output on the oscilloscope terminated in 50ohms. Set the thumbwheel to 9, Mode Switch to “CW” connect the sync output to the horizontal time base of the oscilloscope. The signal on the oscilloscope should be 1/10 the C/2L mode space of the laser. Slow the scope sweep rate to allow 5-10 pulses to appear. The output signal should be jitter-free. Some adjustment of the level control and the threshold control may be required to obtain a jitter free signal. The level control adjusts the Mode Locker electrical input signal level to the frequency doubler. The frequency doubler is sensitive to the input amplitude. In order to obtain the best fundamental suppression, the level control should be adjusted for the best “lock” on the signal being viewed on the oscilloscope. The thumbwheel may be set to the desired division (+1), and the proper output be connected to the drive electronics. The analog output is designed to be used in low division applications. The TTL output for selection rates less than 1MHz. To align the optical “gate” created by the driver/modulator to the laser pulse,
adjust the variable delay control. This control provides a total of 8ns of adjustment. If more is required a fixed 8ns can be added to the variable setting by the fixed 8ns In/Out switch.

**External Input:**
This input may be used for a variety of input signals, most commonly the electrical signal generated by a high-speed photo-detector sampling the optical pulses directly. This input is DC coupled and care must be taken to prevent damage to the sensitive IC’s that are common to this input.

Note: Any signal connected to this input should be viewed on an oscilloscope to verify compliance with the input limits before actual connection is made to the instrument.

**Never exceed +/- 2V DC and AC Combined**

Typically, low level signals (hundreds of milli-volts) will be applied to this input. Photo-detectors that have been mistakenly biased in the forward direction can permanently damage the input comparator and termination.

The external input requires 100mv peak-to-peak input to insure a jitter free trigger. Any typical DC offset and baseline “ring” may be accommodated by the threshold control. This control provides +/- 200mv DC offset to the input comparator. For example, if the detected signal were + 150mv peak with 20-30mv of damped ring on the baseline, the threshold control would typically be adjusted to + 50-60mv to move the trip point of the comparator to a transient free zone. Follow the procedure as outline in the mode locker input to view the analog output. The threshold control should be adjusted for the best hard lock. The external input trips on the leading edge of the signal. This edge should be fast and clean to avoid jitter.
Controls and Indicators

Mode Locker / External Switch:
This switch selects either the Mode Locker input or the external input and directs the signal at their respective BNC connectors to the appropriate electronics on the Front-End PC board. The mode locker input is directed to an amplifier and peak detectors that allow the operator to adjust the level of the signal to the proper operating range. The External input is directed to the input comparator on the Front-End board directly. When the Mode Locker input is selected, the signal at the input is frequency doubled before it reaches the input comparator. The input comparator converts either of the two inputs to ECL logic outputs to run the clock line of the counter.

Level Control:
This control adjusts the level of the signal at the Mode Locker input only. It is not in the circuit when the switch is in External. The level of the signal into the frequency doubler is controlled by this potentiometer. In order to minimize the fundamental output of the doubler, the level into it must be between certain limits. This control will allow the operator to either increase or decrease the signal from the Mode Locker oscillator to best reduce the fundamental “feed-through” of the doubler. The control is adjusted properly when LEVEL LED is green and a jitter free output is obtained from the instrument.

Threshold Control:
This control adjusts the DC bias voltage on the un-driven input (-) of the input comparator. It is in the circuit for both Mode Locker inputs and External Inputs. When the system is being used with the Mode Locker input, this control should be set to mid-range (0v). This control provides a convenient method determining where the input comparator will trip on either the External or Mode Locker input signal. (See figure 1)
In figure 1, the input signal that the system is attempting to lock on has a number of areas where a double or false trigger might occur. At the baseline, ring generated by parasitic resonances in the detector electronics may trigger the counter several times for a single pulse. Also, on the leading edge of the signal, triggering at 60-70mv may generate jitter due to the input window of the comparator. The threshold adjustment allows the comparator’s operating point to be optimized for the desired input signal.
**CW/GATE/S.S. Mode Switch:**

This switch selects the appropriate operating mode for the counter. The CW mode requires no inputs other than the main clock input. It outputs a continuous “string” of pulse whose rate is determined by the setting of the thumbwheel switch and the input clock rate. The Gated mode requires an external TTL timing signal at the Gated input connector. The counter will start operating the first clock pulse after the positive going edge of the gate input signal and continue to run as in the CW mode for as long as this input is held high. The count will terminate one output count after the Gate input goes low. The Single Shot mode also requires an external timing signal. A TTL signal applied to the S.S. input allows the counter to generate a single output pulse at a rate determined by the S.S. source. The positive going edge of this TTL input enables the counter to divide the input clock rate by the setting of the thumbwheel. A single output pulse is generated when the count is reached and the counter resets itself to wait for the next positive edge of the S.S> input signal. This mode allows eternal control of the rate while the thumbwheel sets the incremental delay between the S.S. input and the output pulse.
Figure 3: Gate Mode

Gate Input Signal

Output, Thumbwheel set to 3

Clock Input
Figure 4: S.S. Mode

S.S. Input

Output, Thumbwheel set to 6

S.S. Mode
**Thumbwheel Switch:**
The thumbwheel loads the counter to the number selected on the six decade switch plus one (+1) count. The decoder automatically detects if a difference exists between the number on the thumbwheel and the binary input to the counter. If an error exists, the right count is loaded. When a change is made to the thumbwheel, the counter is inhibited until the new number is loaded.

**Reset Push Button:**
Simply resets the decoder to the number present on the thumbwheel.

**Counting LED:**
This indicator is illuminated when the counter is running. The drive for this function is obtained at the output end of the countdown/delay chain. It will operate only if pulses are being delivered to the output drivers. This indicator provides a convenient means of determining if the input clock to the system is of sufficient amplitude and pulse width to operate the clock line of the counter.

**Delay Controls:**
The variable delay knob controls the setting of a 7bit digital delay line. It has a range of 0 to >8ns in 62ps steps. This feature adds delay to the intrinsic propagation delay of the counter and its output stages. The LOCK and UNLOCK illuminated pushbuttons simply latch or unlatch the binary setting into the delay chips. When the delay is locked, any jitter that might be generated by the LSB’s of the 7bit work are latched. The fixed 8ns IN/OUT delay provides a greater total delay range. This delay is added before the output sync signal picked off to reduce the overall delay between sync and output.
Inputs and Outputs

Inputs:
Mode Locker input is designed to accept the sinusoidal output of the mode locker oscillator, frequency double it and convert it to ECL logic levels to drive the clock line of the counter. An adjustment control is provided (level) to bring the oscillator signal with the desired limits of the frequency doubler. In order to minimize the fundamental (F) feed through of the doubler (2F), the level into it must be between certain limits. Excessive Fundamental feed through will place AM modulation on the doubled output and may cause the input comparator to generate some jitter on the clock line. By frequency doubling this input, correlation between the selected setting of the thumbwheel and the output rate of the counter is maintained. Input amplitude of the mode locker signal should be between -6dbm and +15dbm for proper operation. This input is DC coupled to the 50ohm termination, any DC terms in the output of the mode locker oscillator should be removed before connection is made to the instrument.

External:
The External input provides a direct path to the non-inverting input of the input comparator. This input is DC coupled to the 50ohm termination and the (+) input of the comparator. The comparator has a 30mv window (uncertainty) between its inverting and non-inverting inputs. This device is capable of operating well over 500MHz and will trip on transients in the input waveform if care is not taken to insure the input signal is free of undesirable responses. The inverting (-) terminal of the comparator is controlled by the threshold control, providing DC bias voltage to the device. This bias voltage allows the 30mv “window” of the comparator to be moved to a position on the input waveform most desirable for triggering the clock line of the counter. This input will accept a positive or negative going signal but the clock is always generated by the positive going edge the waveform. The mode locker oscillator signal may be applied to this input if desired. Care should be exercised at this input to insure combined DC and AC signals do not exceed +/- 2v about ground. Pulse width of the input signal at the trip point should be in the order of 1-to-1.5ns for proper clocking of the counter.

Gate:
This input accepts TTL levels and is terminated in 50ohms to ground. If this input is to be driven from TTL logic, a “74S140” 50ohm line driver is recommended.

Single Shot:
Same as input levels of Gate (see above).
**Single Shot Pushbutton:**
This manual input is wired with the BNC single shot in and has its own internal one shot pulse generator.

**Analog Output:**
This output is designed to drive high frequency linear RF Power Amplifiers. The ECL signal at the end of the countdown and the delay chain is level shifted and amplified slightly to provide a unipolar 0 to +1v pulse out into a 50ohm DC load to ground. The pulse width of this signal is determined by a length of 50ohm coax used as a delay line in a D type flip-flop after the delay chips. The width of this pulse may be altered by either increasing or decreasing the length of this line. The pulse width will be fixed by this delay element so high output rates (low division) may not be attainable if the pulse width is made too long. With the standard 8ns width, the analog out will run to the limit of the instrument (140MHz/2). Rise and Fall times are in the order of 2ns.

**TTL:**
This output is a 50hm TTL line driver designed to drive avalanche or HV Mosfet type drivers with 50ohm input impedance. The output pulse width of this signal is set internally by discrete components and is in the order of 800ns. The pulse width may be altered by changing these components down to a minimum of approximately 50ns. If the countdown rate is such that the output signal is in excess of 1MHz, the output will stay logic high.

**Sync:**
This output is intended to be used for oscilloscope horizontal time base trigger. The source for this output is the countdown signal before the variable delay line and after the fixed delay (if selected). The negative edge of the signal should be used for sync as the positive going edge will be delayed in time as a function of the clock input rate. This output will deliver 1.2v into an open circuit, .6v if the sync line is terminated in 50ohms at the oscilloscope.